WHAT IS CLAIMED IS:

1. A method of optimizing a circuit design model during logic synthesis, comprising:

creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design; and

using the structural metric during logic synthesis to create an optimized circuit design model.

2. The method of claim 1, wherein using the structural metric during logic synthesis to create an optimized circuit design model comprises adding, deleting or substituting one or more circuits using a combination of boolean, algebraic and electrical optimizations to create an optimized circuit design model.

3. The method of claim 1, wherein creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design comprises creating a structural metric prior to physical design, the structural metric when applied to a graph of the circuit design model is directly proportional to a routing congestion of the circuit design model after placement and routing, the routing congestion being measured by an average and a peak number of wires crossing any bisection of the placed and routed circuit design model.

4. The method of claim 1, wherein using the structural metric during logic synthesis comprises using the structural metric during a technology independent synthesis stage of the logic synthesis.

5. The method of claim 1, wherein using the structural metric during logic synthesis comprises using the structural metric during the technology mapping stage of the logic synthesis.

6. The method of claim 1, wherein using the structural metric during logic synthesis comprises using the structural metric during the buffering stage of the logic synthesis.

7. The method of claim 1, further comprising incrementally updating the structural metric when logic changes are made to the circuit design model.

8. The method of claim 1, wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises performing recomputation on circuits involved in an optimization and circuits affected by the optimization to provide a structural metric cost.

9. The method as in claim 1, wherein incrementally updating the structural metric when logic changes are made to the circuit design model comprises maintaining information regarding circuits affected by an optimization, which are computed when recomputation of the structural metric is necessary.

10. The method of claim 1, wherein creating the structural metric comprises creating any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric.

11. The method of claim 1, wherein creating a structural metric comprises:

generating one or more possible optimizations;

incrementally updating the structural metric when the optimizations are made to the circuit design model to evaluate the cost of applying each of the one or more possible optimizations to the circuit design model, the structural metric comprising any one of a distance metric, a sum-of-all-pairs-min-cut ("SAPMC"), and an expansion metric;

evaluating a structural metric cost of each of the one or more possible optimizations as given by the structural metric;

selecting an optimization from the one or more possible optimizations with the lowest structural metric cost; and

applying the optimization to the circuit design model.

12. The method of claim 11, wherein generating the one or more possible optimizations comprises:

generating a structure-driven kernel factoring;

generating a structure-driven decomposition;

generating a structure-driven tech mapping; and

generating a structure-aware buffering.

13. A machine-readable medium having instructions stored thereon for optimizing a circuit design model during logic synthesis, comprising the steps of:

creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design; and

using the structural metric during logic synthesis to create an optimized circuit design model.

14. A system for optimizing a circuit design model during logic synthesis, comprising:

means for creating a structural metric prior to physical design, the structural metric being proportional to the routability of the circuit design model after the physical design; and

means for using the structural metric during logic synthesis to create an optimized circuit design model.